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(54) RADIATION IMAGINGING SYSTEM

BILDWANDLERSYSTEM

SYSTEME D'IMAGERIE PAR RAYONNEMENT

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Description

[0001] This invention relates in general to radiation imaging systems, and more particularly but not exclusively to an X-ray imaging panel incorporating a capacitive coupling radiation detector and a reset switch for periodically resetting the potential of the capacitive radiation detector.

[0002] Amorphous selenium (a-Se) has recently been recognized as a promising material for digital X-ray imaging devices for medical and industrial applications. One such prior art device has been described in a paper entitled "A Large Area Solid-State Detector for Radiology Using Amorphous Selenium", Medical Imaging VI: Instrumentation SPIE 1651, pages 134-143 (1992). This article describes a digital X-ray imaging device in which a high voltage is applied to a selenium (Se) plate to obtain high conversion efficiency of X-rays. Depending on the thickness of the Se film, the DC bias voltage may be over several thousand volts. The use of high voltage on the Se film poses serious risks to any semiconductor device connected to the X-ray conversion plate.

[0003] One approach to avoiding such risks involves separating the high voltage parts from the signal detection circuits by inserting an insulator between the readout circuit and Se film. X-ray imaging devices comprising an Se film and insulator (electrode/Se/insulator/readout circuit or readout circuit/Se/insulator/electrode) are described in a paper entitled "A Method of Electronic Readout of Electrophotographic and Electroradiographic Images" D.M. Korn et al, Journal of Applied Photographic Engineering vol. 4, no. 4, Fall 1978, and a paper entitled " Laser Readout of Electrostatic Images", by A Zermeno at al, SPIE vol. 173, Application of Optical Instrumentation and Medicine VII, pages 81-87 (1979). Furthermore, U.S. Patent 5,017,989 (R.A. Street), issued to Xerox Corporation, discloses a configuration of electrode/Se/insulator/readout circuits. In this prior art patent, an improvement is identified in the use of a thin film transistor (TFT) circuit which is overlaid on the insulation film to amplify and output the imaging signal. US-A-5017989 corresponds to the preamble of claim 1.

[0004] In the prior art devices referred to above, a signal voltage is capacitively coupled to the readout circuit. Thus, the readout circuit is not capable of resetting The potential of the Se film automatically (i.e. non-destructive readout). After readout, the bias voltage of the Se film must be inverted, in order to make the signal charge reverse, Thereby resetting the potential of the Se film and preparing The panel for the next X-ray exposure.

[0005] A significant disadvantage of each of the above-referenced prior art devices is that they are substantially incapable of performing real-time acquisition of X-ray images (i.e. incapable of attaining high speed operation to obtain a video rate signal (e.g. 30 frames/second)).

[0006] This disadvantage is caused by two reasons which are discussed in greater detail below under the heading "Detailed Description of The Preferred Embodiment and Further Description of the Prior Art".

[0007] According to the invention there is provided a radiation imaging system as outlined in claim 1.

[0008] In the preferred embodiment, the pixels of said array are arranged in rows and columns, the pixels of each row being interconnected by the control lines and the pixels of each column being interconnected by the data lines, the control lines being arranged to actuate the readout switch means of the pixels of said rows, and the data lines being arranged to receive charges output from the readout switch means of the pixels of said columns.

[0009] Operation of such a radiation imaging system preferably comprises the sequence of steps as outlined in claim 25.

[0010] Moreover, in the preferred embodiment, control signals are applied to successive ones of the control lines for transferring charges from successive rows of the pixels onto the data lines, the control signals serving also to actuate the reset switch means of rows of pixels that have already been read out to which the control line concerned is connected, wherein, after read out of all of said rows of pixels, control signals are applied simultaneously to all of said control lines to actuate all of said readout switch means and reset switch means simultaneously.

[0011] As a consequence it is possible to design a radiation imaging system (e.g. panel) that can provide signal readout with high sensitivity and high speed response, in contrast with the above-described prior art, thus to allow real-time imaging. Furthermore, by incorporating a reset circuit with high voltage and large current tolerance, reliability of circuit operation can be enhanced.

[0012] For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:-

Figure 1 is a graph showing photocurrent and dark current versus bias voltage applied across an Se film as known from the prior art;

Figure 2 is a schematic diagram of an equivalent circuit of a single pixel of an imaging array according to embodiments of the present invention;

Figure 3 is a schematic diagram of an imaging sensor array incorporating multiple pixels in accordance with an embodiment of the present invention;

Figure 4 is a schematic layout of a single pixel according to the preferred embodiment;

Figure 5 is a cross-section through the line A-B in Figure 4;

Figure 6 is a cross-section view of a single pixel according to a first alternative embodiment of the

invention;

Figure 7 is a cross-section view of a single pixel according to a second alternative embodiment of the invention;

Figure 8 is a cross-section view of a single pixel according to a third alternative embodiment of the invention;

Figure 9 is a cross-section view of a single pixel according to a fourth alternative embodiment of the invention;

Figure 10 is a schematic diagram of a sensor array according to a further alternative embodiment; and

Figure 11 is a timing diagram for the sensor array shown in Figure 3.

[0013] As discussed above, certain prior art digital X-ray imagers suffer from the disadvantage that they are incapable of attaining sufficiently high speed for real-time acquisition of X-ray images. There are two causes for this disadvantage in this prior art. Firstly, with reference to Figure 1, a plot is provided of dark current and photocurrent versus bias voltage applied across an Se film, from which it will be noted that both photocurrent and dark current decrease dramatically with a decrease of bias voltage across the Se film. This suggests that a long time is required in order to discharge the Se film completely, or else a large decay-lag results. This characteristic is more serious in the case of low-dose X-rays, such as experienced during X-ray fluoroscopy or X-ray television. Secondly, it is difficult with the Se bias voltage circuit to switch the high bias voltage, e.g. from 2000V to -2000V at the video frequency of 30Hz without introducing additional electronic noise or air discharging problems. Moreover, the high voltage pulse will feed into the signal readout circuits through the insulator. This is because the insulator inserted between the Se film and the readout circuits in prior art systems can only insulate the readout circuits from the electrostatic field or DC component of the electric field, and cannot insulate the readout circuits from electric fields that change with time (i.e. the AC component of the electric field). Therefore, the bias voltage on the Se film in such prior art devices must be changed slowly in order to reduce the differential voltage. Operating prior art devices in this fashion increases the response time.

[0014] Figure 2 depicts an equivalent circuit of a single pixel in an X-ray imaging array according to the embodiments of the present invention described further below. The circuit comprises a readout switch 1 having a control terminal connected to one of a plurality of parallel control lines 7, an output terminal connected to one of a plurality of parallel data lines 6, and an input terminal connected to a storage capacitor 2 having capacitance Cs. The storage capacitor 2 is connected in turn to a radiation detector 4 and a reset switch 3. Where the radiation detector 4 comprises a thick film of Se, as in the preferred embodiment discussed in greater detail below, the capacitance may be represented as Cse.

[0015] In operation, a bias voltage is applied to the radiation detector 4 such that when exposed to radiation (e.g. X-rays), electrical charges (e.g. electrons and holes) are generated in the radiation detector and stored on capacitor 2. A vertical scanner (Figure 3) generates control signals on successive ones of the control lines 7 for actuating successive rows of the readout switches of an array of pixels (e.g. Figure 3), for discharging successive rows of the storage capacitors 2. The signal charge from each capacitor 2 is applied to a data line 6 for subsequent readout, as discussed in greater detail below with reference to Figure 3.

[0016] The collection efficiency of signal charge is proportional to the ratio of the storage capacitance of capacitor 2 and the capacitance of the radiation detector 4 (i.e. where the radiation detector 4 is fabricated from Se, then the collection efficiency is given by Cs/(Cs+Cse)).

[0017] As discussed above, since the signal voltage is capacitively coupled to the readout switch 1, the readout switch cannot reset the potential of the radiation detector 4 automatically. Thus, in the prior art systems discussed above, the bias voltage applied to the radiation detector 4 is inverted, in order to make the signal charges reverse, thereby resetting the potential of the radiation detector 4 (e.g. Se film).

[0018] However, in the imaging array of Fig. 2, a switch 3 is connected to the radiation detector 4 and storage capacitor 2 for rapidly resetting the potential (i.e. bias voltage) across the radiation detector 4 to a predetermined voltage (e.g. ground or some other suitable reset voltage), thereby facilitating real-time operation of the sensor. As discussed in greater detail below, the switch 3 may be constructed as a TFT, diode, MIM (metal-insulator-metal) or MIS (metal-insulator-semiconductor) switch, or from other suitable switching technology.

[0019] Turning now to Figure 3, a plurality of sensor pixels are shown (i.e. four such pixels are shown in the representative array of Figure 3, although in practice, a typical array would comprise a plurality of pixels arranged in a rectangular array).

[0020] In the embodiment of Figure 3, reset switch 3 is fabricated as a TFT which is connected to one terminal of radiation detector 4 (the other terminal not shown, but overlying the entire sensor array and connected to a source of high DC bias voltage, as discussed in greater detail below with reference to Figures 5-9). The other terminal of each reset switch 3 is connected to a reset source line 5 connected to the reset potential V_R.

[0021] As discussed above, successive ones of control lines 7 are connected to a vertical scanner 8 for generating control pulses on successive ones of the control lines 7, as discussed in greater detail below with reference to Figure 11.

[0022] A read-out circuit is provided in the form of a multiplexer 9 having a plurality of charge integration

amplifiers 14 connected to a plurality of inputs thereof. Each amplifier 14 is connected to one of the data lines 6 of the sensor array, for integrating charge carried by the data lines in a well known manner, and applying an output signal representative thereof to the multiplexer 9. The multiplexer 9 then multiplexes successive rows of the scanned sensors into a serial output stream for subsequent processing (e.g. A/D conversion, digital signal processing, image display, etc.). The operation of the charge integration amplifiers 14, vertical scanner 8 and multiplexer 9 will be well known to a person of ordinary skill in the art.

[0023] Turning now to Figure 11 in conjunction with Figure 3, operation of the sensor array is briefly described. Figure 11 depicts the control signals generated by vertical scanner 8, as well as readout and refresh signals generated by an additional control circuit (not shown, but of standard design). Charges stored on the capacitors 2 are transferred to the data line 6 on a row-by-row basis in response to scanner 8 enabling successive rows of the TFT readout switches 1. Thus, as shown in Figure 11, the first row of readout switches 1 is enabled in response to vertical scanner 8 generating a control pulse (ϕyi).

[0024] The charge transferred from each storage capacitor 2 to the data line 6 is then integrated via the charge integration amplifiers 14 and is applied to multiplexer 9.

[0025] The charges applied to multiplexer 9 by respective ones of the amplifiers 14, are multiplexed and read out of multiplexer 9 in serial format in response to the external controller generating a plurality of successive additional control signals ϕxj, $\phi xj+1$, $\phi xj+2$, etc., so that the image data appearing on each pixel sensor is read out in succession (i.e. serial output). The integration capacitors of charge integration amplifiers 14 are then reset in response to the external control circuit generating a positive refresh pulse signal (ϕr).

[0026] Next, the second row of storage capacitors 2 is discharged in response vertical scanner 8 generating another control pulse ($\phi yi+1$) on the second row of pixel sensors, for transferring charge to the data lines 6, which charges are then integrated via amplifiers 14 and applied to multiplexer 9 for subsequent readout. However, as will be apparent from Figure 3, when the control pulse $\phi yi+1$ is generated, the TFT reset switches 3 are also enabled in the previous row, for resetting the potential of the radiation detectors 4 of the entire previous row.

[0027] Note that the reset action at this time cannot completely refresh the storage capacitor 2, since the TFT switch 1 of the previous row has turned off, and therefore the terminal of capacitor 2 on switch 1 side is floated electrically and its potential varies with the potential on the opposite terminal. A complete reset operation for the capacitor 2 is carried out after all of the pixels on the imaging panel have been read out.

[0028] This readout and react process continues for all subsequent rows of the sensor array in response to the vertical scanner generating successive additional control pulses (e.g. $\phi yi+2$, etc.) on successive control lines 7 of the array.

[0029] Once vertical scanner 8 has caused charges on each row of the sensor to be readout (i.e. after one frame image), vertical scanner 8 generates a further high voltage level control pulse to all control lines 7, thereby resetting all pixels at one time.

[0030] Turning now to Figures 4 and 5, a layout of one pixel and a cross section through the pixel, respectively, are shown, in accordance with the preferred embodiment.

[0031] As discussed above with reference to Figures 2 and 3, the sensor array is defined by a plurality of rows of control lines 7 (represented in Figure 4 by gate bus lines 70), and a plurality of columns of data lines 6. The lines 70 and 6 are preferably fabricated from Cr, in the usual manner. The gate lines 70 are deposited on a glass substrate 10 with individual gates 73 extending into the active pixel area. A layer of insulator 11 (e.g. SiO_2 or a-SiN) is deposited over the gate 73 and substrate 10. Individual Cr gates 72 of the reset switch 3 are deposited on the insulation layer 11 and contact the control lines 70 via contact vias 71.

[0032] A layer of CdSe semiconductor 12 is deposited on insulation layer 11 so as to overlay the gate 73 of readout switch 1. Data lines 6 (also fabricated from Cr) and lower pixel electrodes 21 (also fabricated from Cr) are deposited on insulating layer 11 so as to contact the semiconductor region 12. A further insulation layer 20 of a-SiN is deposited over the gate 72 of reset switch 3, data line 6, semiconductor region 12, lower pixel electrode 21 and the underlying insulation layer 11.

[0033] Source line 5 for the reset switch 3 and upper pixel electrode 22 are then deposited on the insulating layer 20, and a further semiconductor region 30 (preferably CdSe) is deposited so as to contact source line 5 and upper pixel electrode 22, and so as to be substantially aligned with the gate 72 of reset switch 3.

[0034] Next, a layer 40 of a a-Se is deposited over the entire array, followed by a blocking layer 41 of CeO_2 and an upper electrode or contact 42 of Al which, in combination with upper pixel electrode 22, is used to apply a high DC bias voltage to the a-Se layer 40.

[0035] Because the second gate dielectric film 20 (preferably fabricated from a-SiN) is made thick (e.g. 500 nm to 1000 nm) with high permittivity (e.g. approximately 9), the breakdown voltage between the pixel electrode 22 and the TFT readout switch 1 is extremely high.

[0036] As discussed above, the collection efficiency of signal charge is given by Cs/(Cs+Cse). Because the thickness of the Se film 40 for radiation detection can be on the order of 300 μm, over 98% of signal charge can be readout.

[0037] The TFT structure shown in Figures 4 and 5 is just one of a number of various TFT structures which

are suitable for embodying the present invention.

[0038] Figures 6, 7, and 8 show cross-sectional views with different structure of the reset TFT 3. Reference numerals which are common to Figures 5-8 represent common features. Thus, in the alternative embodiment of Figure 6, a TFT reset switch 3 is fabricated using a semiconductor layer 32 of a-Se + As_2Se_3. In the embodiment of Figure 7, the reset switch 3 is fabricated using a P channel TFT device with semiconductor region 31 of p^+-a-Si, and wherein the semiconductor material 13 for readout switch 1 is fabricated using a-Si. In the embodiment of Figure 8, the reset switch 3 is fabricated as a TFT device, the semiconductor film of radiation conversion 4 is also used for the TFT switch 3. The semiconductor region 13 of readout switch 1 being fabricated from a-Si, as is the radiation detection film 44.

[0039] Figure 9 shows another structure employing a a-Si p-i-n diode switch as the reset switch 3. The diode comprises a layer 34 of a-Si sandwiched between an anode layer 35 of p^+-a-Si and a cathode layer 36 of n^+-a-Si. The diode is deposited on a reset control line 50 of Cr.

[0040] Figure 10 shows a further alternative embodiment of the invention wherein the source lines 5 for the reset switches 3 are arranged parallel to the gate lines 7.

[0041] This design allows a driving pulse wave, which is synchronous with the gate contral pulse, but with different voltage levels to be applied to the source line 5, in order to increase the on-current and reduce the off-current of the reset switch 3.

[0042] Alternative embodiments and variations are possible. For example, although the embodiments described above refer to a well known multiplexer readout, alternative readout circuits and devices may be utilized, such as a TFT readout array with built-in TFT amplifier in each pixel, laser beam scanning readout, spatial light modulator readout (i.e. light valve) employing liquid crystal or solid-state image intensifiers with electric luminance film, etc.

[0043] One preferred combination is a reset switch 3 comprising an MIM transistor and a TFT read out switch 1 fabricated with an a-Si semiconductor region.

Claims

1. A radiation imaging system comprising a plurality of control lines (7), a plurality of data lines (6) and an array of pixels, each pixel comprising:

   radiation detector means (4) for directly converting incident radiation to electrical charges and capacitively coupled to a readout switch means (1);
   storage capacitor means (2) connected to the radiation detector means (4) for storing charges generated by the radiation detector means (4);
   said readout switch means (1) having a first terminal thereof connected to the storage capacitor means (2), a control terminal thereof connected to first respective ones of said control lines (7) and a second terminal thereof connected to one of said data lines (6) and actuable to transfer charges stored on the storage capacitor means (2) to said data line in response to a control signal on said control line;
   characterised by each of said pixels further comprising reset switch means (3) having a first terminal thereof connected to the said radiation detector means (4), a control terminal thereof connected to further respective ones of said control lines (7) adjacent said first respective ones of said control lines, and a second terminal thereof connected to a source of reset potential (5) and actuable to reset the charge state of the radiation detector means (4) and the storage capacitor means (2).

2. A system according to claim 1, wherein the pixels of said array are arranged in rows and columns, the pixels of each row being interconnected by the control lines (7) and the pixels of each column being interconnected by the data lines (6), the control lines (7) being arranged to actuate the readout switch means (1) of the pixels of said rows, and the data lines (6) being arranged to receive charges output from the readout switch means (1) of the pixels of said columns.

3. A system according to claim 2, wherein each row of pixels is arranged so that the reset switch means (3) and the readout switch means (1) of the row concerned are actuatable via different ones of said control lines (7).

4. A system according to claim 2 or 3, arranged so that individual ones of the control lines (7) are operable to actuate the readout switch means (1) of one row of pixels as well as the reset switch means (3) of an adjacent row of pixels, whereby one row of pixels can be read out and an adjacent row of pixels reset at the same time.

5. A system according to claim 2, 3 or 4, wherein the reset switch means (3) are connected to reset source lines (5).

6. A system according to claim 2, 3, 4 or 5, wherein the reset source lines (5) are arranged to interconnect columns of pixels.

7. A system according to claim 2, 3, 4 or 5, wherein the reset source lines (5) are arranged to interconnect rows of pixels.

8. A system according to any one of claims 2 to 7 and comprising scanner means (8) for generating a succession of control signals on successive ones of said control lines (7).

9. A system according to any one of claims 2 to 7 and comprising multiplexer means (9) for receiving charges from said data lines (6) and outputting them in sequence.

10. A system according to any one of the preceding claims, wherein the radiation detector means (4) comprises a semiconductor film (40; 44) extending over the array of pixels and means (42, 22) for applying a high-voltage DC bias voltage to the film (40; 44) at each of said pixels.

11. A system according to claim 10, wherein the bias voltage applying means comprises a first biasing electrode (42) extending over the array of pixels on an upper side of the film (40; 44) and respective second biasing electrodes (22) arranged on an under-side of the film (40; 44), one for each pixel.

12. A system according to claim 10 or 11, wherein the semiconductor film is an a-Se film (40).

13. A system according to claim 10 or 11, wherein the semiconductor film is an a-Si film (44).

14. A system according to claim 10, 11, 12 or 13, wherein each of said storage capacitor means (2) comprises:

a first electrode (22) adjacent said film (40; 44);
a second electrode (21) facing the first electrode (22); and
a dielectric layer (20) between said first electrode (22) and said second electrode (21).

15. A system according to claim 14 when appended to claim 11, wherein, for each pixel, said second electrode and said second biasing electrode are the same electrode (22).

16. A system according to any one of the preceding claims, wherein each of said readout switch means (1) comprises a thin film transistor.

17. A system according to claim 16 when appended to claim 14, wherein, for each readout switch means (1), the thin film transistor thereof has a drain terminal connected to said second electrode (21), a source terminal connected to one of said data lines (6) and a gate terminal (73) connected to one of said control lines (7).

18. A system according to any one of the preceding claims, wherein each of said reset switch means (3) comprises a thin film transistor.

19. A system according to claim 18 when appended to claim 14, wherein, for each reset switch means (3), the thin film transistor thereof has a drain terminal connected to said first electrode (22), a source terminal connected to one of said reset switch source lines (5) and a gate terminal (72) connected to one of said control lines (7).

20. A system according to any one of claims 1 to 17, wherein each of said reset switch means (3) comprises a diode, one terminal of the diode constituting both the control terminal and the second terminal of the reset switch means.

21. A system according to claim 20 when appended to claim 14, wherein, for each reset switch means (3), the diode thereof has an anode (35) connected to said first electrode (22) and a cathode (36) connected to one of said control lines (50).

22. A system according to claim 20 or 21, wherein said diode is an amorphous silicon p-i-n diode.

23. A system according to any one of claims 1 to 17, wherein each of said reset means (3) comprises a metal-insulator-metal transistor.

24. A system according to any one of claims 1 to 17, wherein each of said reset means (3) comprises a metal-insulator-semiconductor transistor.

25. A method of operating a radiation imaging system according to any one of the preceding claims, the method comprising the following sequence of steps being applied to each pixel:

(a) applying a bias voltage to the radiation detector means (4) to cause charges generated in the radiation detector means (4) to be collected on the storage capacitor means (2);
(b) applying a first control signal (ϕyi) to actuate the readout switch means (1) to output charges stored on the storage capacitor means (2);
(c) applying a second control signal ($\phi yi+1$) to actuate the reset switch means (3) to reset charges that remain on the radiation detector means (4) and on the storage capacitor means (2) after charge output through the readout switch means (1) in step (b); and
(d) applying first and second control signals (ϕyi and $\phi yi+1$) together to actuate the readout switch means (1) and the reset switch means (3) simultaneously, to reset charges that still remain on the radiation detector means (4) and on the storage capacitor means (2) after step

(c).

26. A method according to claim 25 when appended to claim 2, wherein control signals are applied to successive ones of the control lines (7) for transferring charges from successive rows of the pixels onto the data lines (6), the control signals serving also to actuate the reset switch means (3) of rows of pixels that have already been read out to which the control line concerned is connected, wherein, after read out of all of said rows of pixels, control signals are applied simultaneously to all of said control lines (7) to actuate all of said readout switch means (1) and reset switch means (3) simultaneously.

Patentansprüche

1. Strahlungs-Bildgebersystem, umfassend eine Anzahl Steuerleitungen (7), eine Anzahl Datenleitungen (6) und eine Pixelanordnung, wobei jedes Pixel umfasst:

   eine Strahlungserfassungsvorrichtung (4), die einfallende Strahlung direkt in elektrische Ladungen umwandelt, und die kapazitiv mit einer Ausleseschaltervorrichtung (1) gekoppelt ist;
   eine Speicherkondensatorvorrichtung (2), die mit der Strahlungserfassungsvorrichtung (4) verbunden ist und Ladungen speichert, die die Strahlungserfassungsvorrichtung (4) erzeugt,
   wobei ein erster Anschluss der Ausleseschaltervorrichtung (1) mit der Speicherkondensatorvorrichtung (2) verbunden ist, ein Steueranschluss der Vorrichtung (1) mit einer ersten entsprechenden Steuerleitung (7) verbunden ist, und ein zweiter Anschluss der Vorrichtung (1) mit einer der Datenleitungen (6) verbunden und so betreibbar ist, dass auf der Speicherkondensatorvorrichtung (2) gespeicherte Ladungen abhängig von einem Steuersignal auf der Steuerleitung auf die Datenleitung übertragen werden,
   dadurch gekennzeichnet, dass jedes Pixel zudem eine Rücksetzschaltervorrichtung (3) umfasst, wobei ein erster Anschluss der Vorrichtung (3) mit der Strahlungserfassungsvorrichtung (4) verbunden ist, ein Steueranschluss der Vorrichtung (3) mit einer weiteren entsprechenden Steuerleitung (7) benachbart der ersten entsprechenden Steuerleitung verbunden ist, und ein zweiter Anschluss der Vorrichtung (3) mit einer Rücksetzpotentialquelle (5) verbunden und die Vorrichtung (3) so betreibbar ist, dass der Ladungszustand der Strahlungserfassungsvorrichtung (4) und der Speicherkondensatorvorrichtung (2) zurückgesetzt wird.

2. System nach Anspruch 1, wobei die Pixel der Anordnung in Zeilen und Spalten angeordnet sind, und die Pixel einer jeden Zeile über die Steuerleitungen (7) verbunden sind, und die Pixel einer jeden Spalte durch die Datenleitungen (6) verbunden sind, und die Steuerleitungen (7) so angeordnet sind, dass sie die Ausleseschaltervorrichtungen (1) der Pixel der Zeilen betätigen, und die Datenleitungen (6) so angeordnet sind, dass sie die Ladungen aufnehmen, die die Ausleseschaltervorrichtungen (1) der Pixel in den Spalten abgeben.

3. System nach Anspruch 2, wobei jede Pixelzeile so angeordnet ist, dass die Rücksetzschaltervorrichtung (3) und die Ausleseschaltervorrichtung (1) der betreffenden Zeile über verschiedene Steuerleitungen (7) ansprechbar sind.

4. System nach Anspruch 2 oder 3, so angeordnet, dass einzelne Steuerleitungen (7) betreibbar sind zum Betätigen der Ausleseschaltervorrichtungen (1) einer Pixelzeile und auch der Rücksetzschaltervorrichtungen (3) einer benachbarten Pixelzeile, so dass gleichzeitig eine Pixelzeile ausgelesen und eine benachbarte Pixelzeile zurückgesetzt werden kann.

5. System nach Anspruch 2, 3 oder 4, wobei die Rücksetzschaltervorrichtungen (3) mit den Rücksetzquellenleitungen (5) verbunden sind.

6. System nach Anspruch 2, 3, 4 oder 5, wobei die Rücksetzquellenleitungen (5) so angeordnet sind, dass sie Pixelspalten verbinden.

7. System nach Anspruch 2, 3, 4 oder 5, wobei die Rücksetzquellenleitungen (5) so angeordnet sind, dass sie Pixelzeilen verbinden.

8. System nach irgendeinem der Ansprüche 2 bis 7, zudem umfassend Abtastvorrichtungen (8), die eine Abfolge von Steuersignalen auf aufeinander folgenden Steuerleitungen (7) erzeugen.

9. System nach irgendeinem der Ansprüche 2 bis 7, zudem umfassend Multiplexervorrichtungen (9), die Ladungen aus den Datenleitungen (6) aufnehmen und sie nacheinander ausgeben.

10. System nach irgendeinem der vorhergehenden Ansprüche, wobei die Strahlungserfassungsvorrichtung (4) eine Halbleiterschicht (40; 44) umfasst, die sich über die Pixelanordnung erstreckt, und Vorrichtungen (42, 22), die die Schicht (40; 44) an jedem Pixel mit einer hohen Gleichspannung vorspannen.

11. System nach Anspruch 10, wobei die Vorspan-

nungsanlegevorrichtung eine erste Vorspannelektrode (42) umfasst, die sich auf der Oberseite der Schicht (40; 44) über die Pixelanordnung erstreckt, und jeweils auf der Unterseite der Schicht (40; 44) angeordnete zweite Vorspannelektroden (22) für jedes Pixel.

12. System nach Anspruch 10 oder 11, wobei die Halbleiterschicht eine a-Se-Schicht (40) ist.

13. System nach Anspruch 10 oder 11, wobei die Halbleiterschicht eine a-Si-Schicht (44) ist.

14. System nach Anspruch 10, 11, 12 oder 13, wobei jede Speicherkondensatorvorrichtung (2) umfasst:

eine erste Elektrode (22) benachbart zur Schicht (40; 44);
eine zweite Elektrode (21), die der ersten Elektrode (22) gegenüberliegt; und
eine dielektrische Schicht (20) zwischen der ersten Elektrode (22) und der zweiten Elektrode (21).

15. System nach Anspruch 14 wenn abhängig von Anspruch 11, wobei für jedes Pixel die zweite Elektrode und die zweite Vorspannelektrode die gleiche Elektrode (22) sind.

16. System nach irgendeinem der vorhergehenden Ansprüche, wobei jede Ausleseschaltervorrichtung (1) einen Dünnfilmtransistor enthält.

17. System nach Anspruch 16 wenn abhängig von Anspruch 14, worin in jeder Ausleseschaltervorrichtung (1) der Drainanschluss des Dünnfilmtransistors der Vorrichtung mit der zweiten Elektrode (21) verbunden ist, der Sourceanschluss mit einer der Datenleitungen (6) verbunden ist und der Gateanschluss (73) mit einer der Steuerleitungen (7) verbunden ist.

18. System nach irgendeinem der vorhergehenden Ansprüche, wobei jede Rücksetzschaltervorrichtung (3) einen Dünnfilmtransistor umfasst.

19. System nach Anspruch 18 wenn abhängig von Anspruch 14, wobei in jeder Rücksetzschaltervorrichtung (3) der Drainanschluss des Dünnfilmtransistors der Vorrichtung mit der ersten Elektrode (22) verbunden ist, der Sourceanschluss mit einer der Rücksetzschalter-Quellenleitungen (5) verbunden ist und der Gateanschluss (72) mit einer der Steuerleitungen (7) verbunden ist.

20. System nach irgendeinem der Ansprüche 1 bis 17, wobei jede Rücksetzschaltervorrichtung (3) eine Diode enthält, und ein Anschluss der Diode sowohl den Steueranschluss als auch den zweiten Anschluss der Rücksetzschaltervorrichtung bildet.

21. System nach Anspruch 20 wenn abhängig von Anspruch 14, wobei in jeder Rücksetzschaltervorrichtung (3) die Diode der Vorrichtung eine Anode (35) besitzt, die mit der ersten Elektrode (22) verbunden ist, und eine Kathode (36), die an eine der Steuerleitungen (50) angeschlossen ist.

22. System nach Anspruch 20 oder 21, wobei die Diode eine P-I-N-Diode aus amorphen Silizium ist.

23. System nach irgendeinem der Ansprüche 1 bis 17, wobei jede Rücksetzvorrichtung (3) einen Metall-Isolierschicht-Metall-Transistor enthält.

24. System nach irgendeinem der Ansprüche 1 bis 17, wobei jede Rücksetzvorrichtung (3) einen Metall-Isolierschicht-Halbleiter-Transistor enthält.

25. Verfahren zum Betreiben eines Strahlungs-Bildgebersystems nach irgendeinen der vorhergehenden Ansprüche, wobei das Verfahren die nachstehende Folge von Schritten umfasst, die auf jedes Pixel angewendet werden:

a) Anlegen einer Vorspannung an die Strahlungserfassungsvorrichtung (4), damit sich die in der Strahlungserfassungsvorrichtung (4) erzeugten Ladungen auf der Speicherkondensatorvorrichtung (2) sammeln;
b) Anlegen eines ersten Steuersignals (ϕyi) zum Betätigen der Ausleseschaltervorrichtung (1), damit die auf der Speicherkondensatorvorrichtung (2) gespeicherten Ladungen ausgelesen werden;
c) Anlegen eines zweiten Steuersignals (ϕyi+1) zum Betätigen der Rücksetzschaltervorrichtung (3), damit die Ladungen zurückgesetzt werden, die nach dem Ladungsausgeben über die Ausleseschaltervorrichtung (1) im Schritt b) auf der Strahlungserfassungsvorrichtung (4) und auf der Speicherkondensatorvorrichtung (2) verbleiben; und
d) gemeinsames Anlegen der ersten und zweiten Steuersignale (ϕyi und ϕyi+1) zum gleichzeitigen Betätigen der Ausleseschaltervorrichtung (1) und der Rücksetzschaltervorrichtung (3), damit Ladungen zurückgesetzt werden, die nach dem Schritt c) noch auf der Strahlungserfassungsvorrichtung (4) und der Speicherkondensatorvorrichtung (2) verbleiben.

26. Verfahren nach Anspruch 25 wenn abhängig von Anspruch 2, wobei Steuersignale an aufeinander folgende Steuerleitungen (7) angelegt werden, um

die Ladungen aus aufeinander folgenden Pixelzeilen auf die Datenleitungen (6) zu übertragen, und die Steuersignale auch dazu dienen, die Rücksetzschaltervorrichtung (3) von Pixelzeilen zu betätigen, die bereits ausgelesen worden sind, und an die die betroffene Steuerleitung angeschlossen ist, und wobei nach dem Auslesen aller Pixelzeilen gleichzeitig Steuersignale an alle Steuerleitungen (7) angelegt werden, um alle Ausleseschaltervorrichtungen (1) und Rücksetzachaltervorrichtungen (3) gleichzeitig zu betätigen.

Revendications

1. Système de visualisation de radiation comprenant une pluralité de lignes (7) de commande, une pluralité de lignes (6) de données et un réseau de pixels, chaque pixel comprenant :

   des moyens (4) formant détecteur de radiation pour convertir directement une radiation incidente on charges électriques et couplé de manière capacitive à des moyens (1) formant commutateur de lecture ;
   des moyens (2) formant condensateur de stockage connectés aux moyens (4) formant détecteur de radiation pour stocker des charges générées par les moyens (4) formant détecteur de radiation ;
   lesdits moyens (1) formant commutateur de lecture ayant une première borne de ceux-ci connectée aux moyens (2) formant condensateur de stockage, une borne de commande de ceux-ci connectée aux premières lignes respectives desdites lignes (7) de commande et une deuxième borne de ceux-ci connectée à l'une desdites lignes (6) de données et pouvant être actionnée pour transférer des charges stockées sur les moyens (2) formant condensateur de stockage vers ladite ligne de données en réponse à un signal de commande sur ladite ligne de commande ;
   caractérisé par le fait que chacun desdits pixels comprend on outre des moyens (3) formant commutateur de remise à l'état initial ayant une première borne de ceux-ci connectée auxdits moyens (4) formant détecteur de radiation, une borne de commande de ceux-ci connectée en outre aux lignes respectives desdites lignes (7) de commande adjacentes auxdites premières lignes respectives desdites lignes de commande, et une deuxième borne de ceux-ci connectée à une source de potentiel (5) de remise à l'état initial et pouvant être actionnée pour remettre à l'état initial l'état de charge des moyens (4) formant détecteur de radiation et des moyens (2) formant condensateur de stockage.

2. Système selon la revendication 1, dans lequel les pixels dudit réseau sont agencés an rangées et colonnes, les pixels de chaque rangée étant interconnectés par les lignes (7) de commande et les pixels de chaque colonne étant interconnectés par les lignes (6) de données, les lignes de commande (1) étant agencées pour actionner les moyens (1) formant commutateur de lecture des pixels desdites rangées, et les lignes (6) de données étant agencées pour recevoir des charges délivrées par les moyens (1) formant commutateur de lecture des pixels desdites colonnes.

3. Système selon la revendication 2, dans lequel chaque rangée de pixels est agencée de telle sorte que les moyens (3) formant commutateur de remise à l'état initial et les moyens (1) formant commutateur de lecture de la rangée concernée peuvent être actionnés par l'intermédiaire de différentes lignes desdites lignes (7) de commande.

4. Système selon la revendication 2 ou 3, agencé de telle sorte que des lignes individuelles des lignes (7) de commande peuvent fonctionner pour actionner les moyens (1) formant commutateur de lecture d'une rangée de pixels ainsi que les moyens (3) formant commutateur de remise à l'état initial d'une rangée adjacente de pixels, à la suite de quoi une rangée de pixels peut être lue et une rangée adjacente de pixels remise à l'état initial, en même temps.

5. Système selon la revendication 2, 3 ou 4, dans lequel les moyens (3) formant commutateur de remise à l'état initial sont connectés à des lignes (5) formant source de remise à l'état initial.

6. Système salon la revendication 2, 3, 4 ou 5, dans lequel les lignes (5) formant source de remise à l'état initial sont agencées pour interconnecter des colonnes de pixels.

7. Système selon la revendication 2, 3, 4 ou 5, dans lequel les lignes (5) formant source de remise à l'état initial sont agencées pour interconnecter des rangées de pixels.

8. Système selon l'une quelconque des revendications 2 à 7 et comprenant un moyen (8) formant dispositif de balayage pour générer une succession de signaux de commande sur des lignes successives desdites lignes (7) de commande.

9. Système selon l'une quelconque des revendications 2 à 7 et comprenant un moyen (9) formant multiplexeur pour recevoir des charges en provenance desdites lignes (6) de données et les délivrer en séquence.

10. Système selon l'une quelconque des revendications précédentes, dans lequel les moyens (4) formant détecteur de radiation comprennent un film (40 ; 44) semiconducteur s'étendant sur le réseau de pixels et un moyen (42, 22) pour appliquer une haute tension de polarisation en courant continu au film (40 ; 44) au niveau de chacun desdits pixels.

11. Système selon la revendication 10, dans lequel le moyen d'application de tension de polarisation comprend une première électrode (42) de polarisation s'étendant sur le réseau de pixels sur une face de dessus du film (40 ; 44) et des deuxièmes électrodes de polarisation respectives (22) agencées sur une face de dessous du film (40 ; 44), à raison d'une pour chaque pixel.

12. Système selon la revendication 10 ou 11, dans lequel le film semiconducteur est un film de a-Se (40).

13. Système selon la revendication 10 ou 11, dans lequel le film semiconducteur est un film de a-Si (44).

14. Système selon la revendication 10, 11, 12 ou 13, dans lequel chacun desdits moyens (2) formant condensateur de stockage comprend :

    une première électrode (22) adjacente audit film (40 ; 44) ;
    une deuxième électrode (21) faisant face à la première électrode (22) ; et
    une couche diélectrique (20) entre ladite première électrode (22) et ladite deuxième électrode (21).

15. Système selon la revendication 14 lorqu'elle dépend de la revendication 11, dans lequel, pour chaque pixel, ladite deuxième électrode et ladite deuxième électrode de polarisation sont la même électrode (22).

16. Système selon l'une quelconque des revendications précédentes, dans lequel chacun desdits moyens (1) formant commutateur de lecture comprend un transistor à film mince.

17. Système selon la revendication 16 lorsqu'elle dépend de la revendication 14, dans lequel, pour chaque moyen (1) formant commutateur de lecture, le transistor à film mince de celui-ci a une borne de drain connectée à ladite deuxième électrode (21), une borne de source connectée à l'une desdites lignes (6) de données et une électrode de grille (73) connectée à l'une desdites lignes (7) de commande.

18. Système selon l'une quelconque des revendications précédentes, dans lequel chacun desdits moyens (3) formant commutateur de remise à l'état initial comprend un transistor à film mince.

19. Système selon la revendication 18 lorsqu'elle dépend de la revendication 14, dans lequel, pour chaque moyen (3) formant commutateur de remise à l'état initial, le transistor à film mince de celui-ci a une borne de drain connectée à ladite première électrode (22), une borne de source connectée à l'une desdites lignes (5) formant source de commutateur de remise à l'état initial et une borne de grille (72) connectée à l'une desdites lignes (7) de commande.

20. Système selon l'une quelconque des revendications 1 à 17, dans lequel chacun desdits moyens (3) formant commutateur de remise à l'état initial comprend une diode, une borne de la diode constituant à la fois la borne de commande et la deuxième borne du moyen formant commutateur de remise à l'état initial.

21. Système selon la revendication 20 lorsqu'elle dépend de la revendication 14, dans lequel, pour chaque moyen (3) formant commutateur de remise à l'état initial, la diode de celui-ci a une anode (35) connectée à ladite première électrode (22) et une cathode (36) connectée à l'une desdites lignes (50) de commande.

22. Système selon la revendication 20 ou 21, dans lequel ladite diode est une diode p-i-n au silicium amorphe.

23. Système selon l'une quelconque des revendications 1 à 17, dans lequel chacun desdits moyens (3) de remise à l'état initial comprend un transistor métal-isolant-métal.

24. Système selon l'une quelconque des revendications 1 à 17, dans lequel chacun desdits moyens (3) de remise à l'état initial comprend un transistor métal-isolant-semiconducteur.

25. Procédé de mise en oeuvre d'un système de visualisation de radiation selon l'une quelconque des revendications précédentes, le procédé comprenant la séquence d'étapes suivante destinée à être appliquée à chaque pixel :

    (a) application d'une tension de polarisation aux moyens (4) formant détecteur de radiation pour conduire des charges, générées dans les moyens (4) tonnant détecteur de radiation, à être collectées sur las moyens (2) formant condensateur de stockage ;

(b) application d'un premier signal de commande (ϕyi) pour actionner les moyens (1) formant commutateur de lecture pour délivrer des charges stockées sur les moyens (2) formant condensateur de stockage ;

(c) application d'un deuxième signal de commande ($\phi yi + 1$) pour actionner les moyens (3) formant commutateur de remise à l'état initial pour remettre à l'état initial des charges qui restent sur les moyens (4) formant détecteur de radiation et sur les moyens (2) formant condensateur de stockage après la délivrance de charge par l'intermédiaire des moyens (1) formant commutateur de lecture au cours de l'étape (b) ; et

(d) application de premier et deuxième signaux de commande (ϕyi et $\phi yi + 1$), ensemble, pour actionner simultanément les moyens (1) formant commutateur de lecture et les moyens (3) formant commutateur de remise à l'état initial, pour remettre à l'état initial des charges qui restent encore sur les moyens (4) formant détecteur de radiation et sur les moyens (2) formant condensateur de stockage après l'étape (c).

26. Procédé selon la revendication 25 lorsqu'elle dépend de la revendication 2, dans lequel des signaux de commande sont appliqués à des lignes successives des lignes (7) de commande pour transférer des charges depuis des rangées successives de pixels sur les lignes (6) de données, les signaux de commande servant aussi à actionner les moyens (3) formant commutateur de remise à l'état initial de rangées de pixels qui ont déjà été lues auxquelles est connectée la ligne de commande concernée, dans lequel, après lecture de la totalité desdites rangées de pixels, des signaux de commande sont appliqués simultanément à la totalité desdites lignes (7) de commande pour actionner simultanément la totalité des moyens (1) formant commutateur de lecture et des moyens (3) formant commutateur de remise à l'état initial.

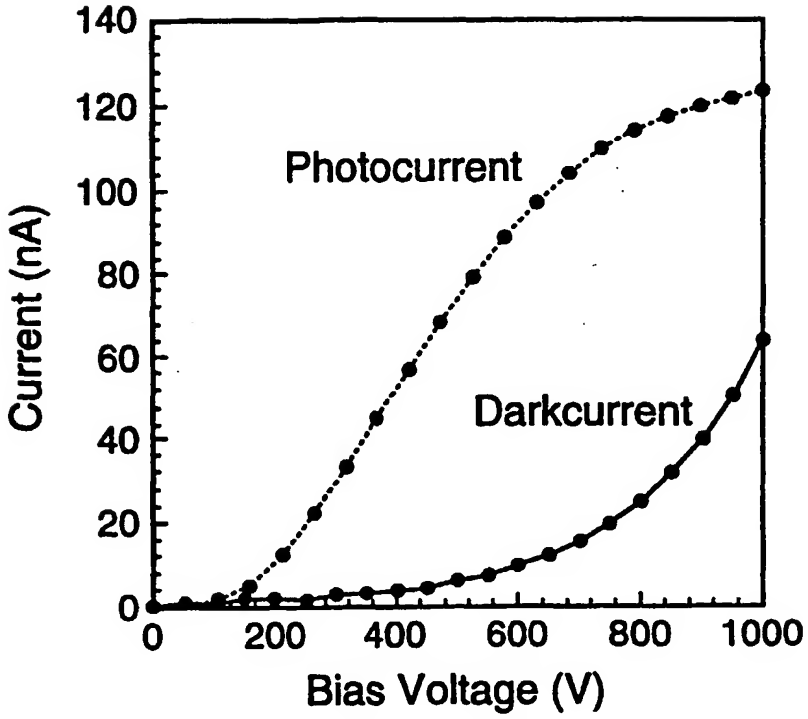

FIG.1. PRIOR ART

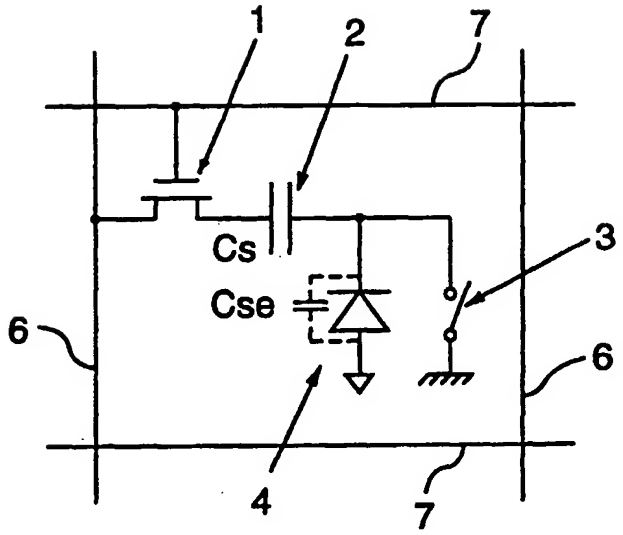

FIG.2.

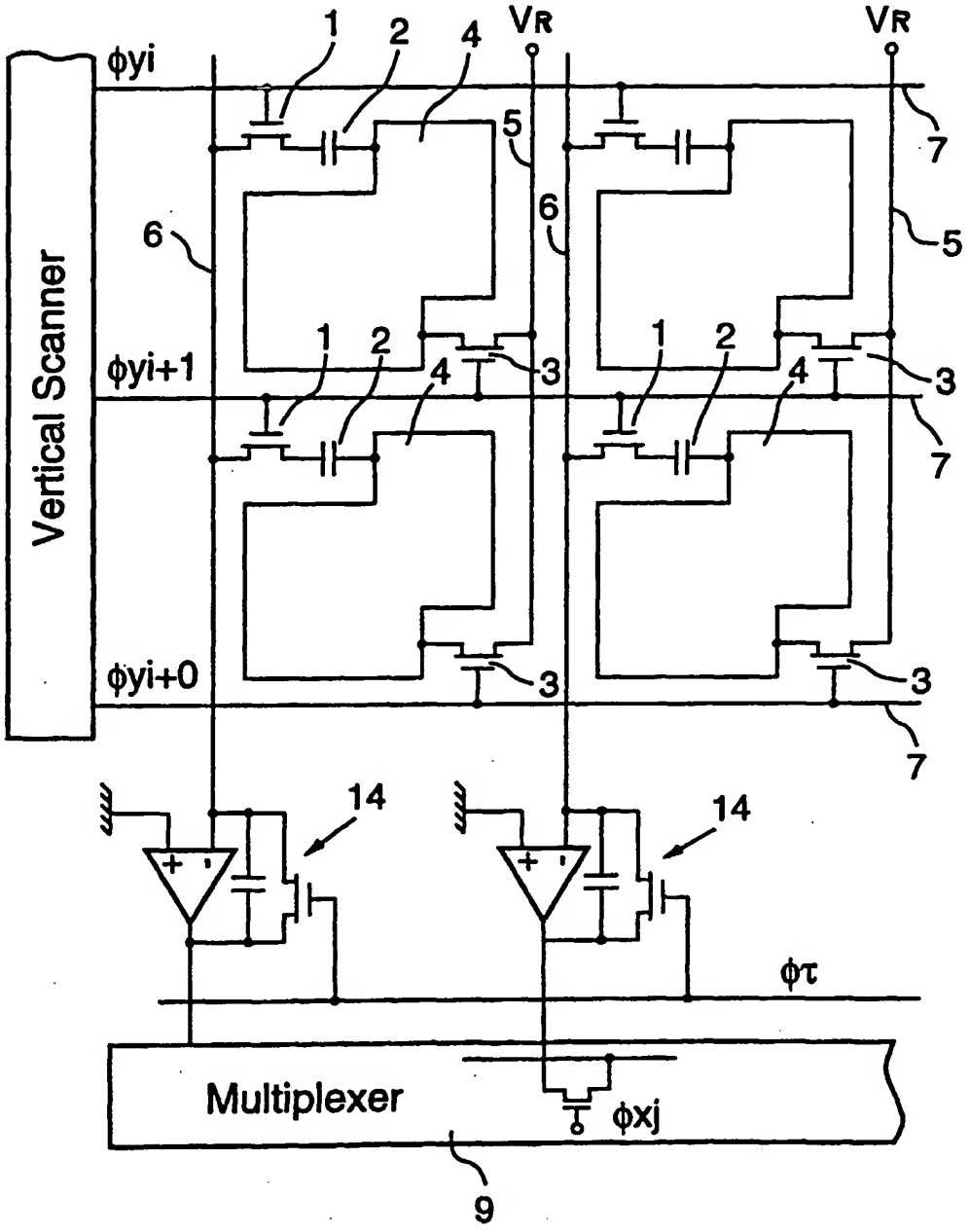
Vertical Scanner
φyi
φyi+1
φyi+0
1
2
4
3
5
6
7
VR
14
φτ
Multiplexer
φxj
9

FIG.3.

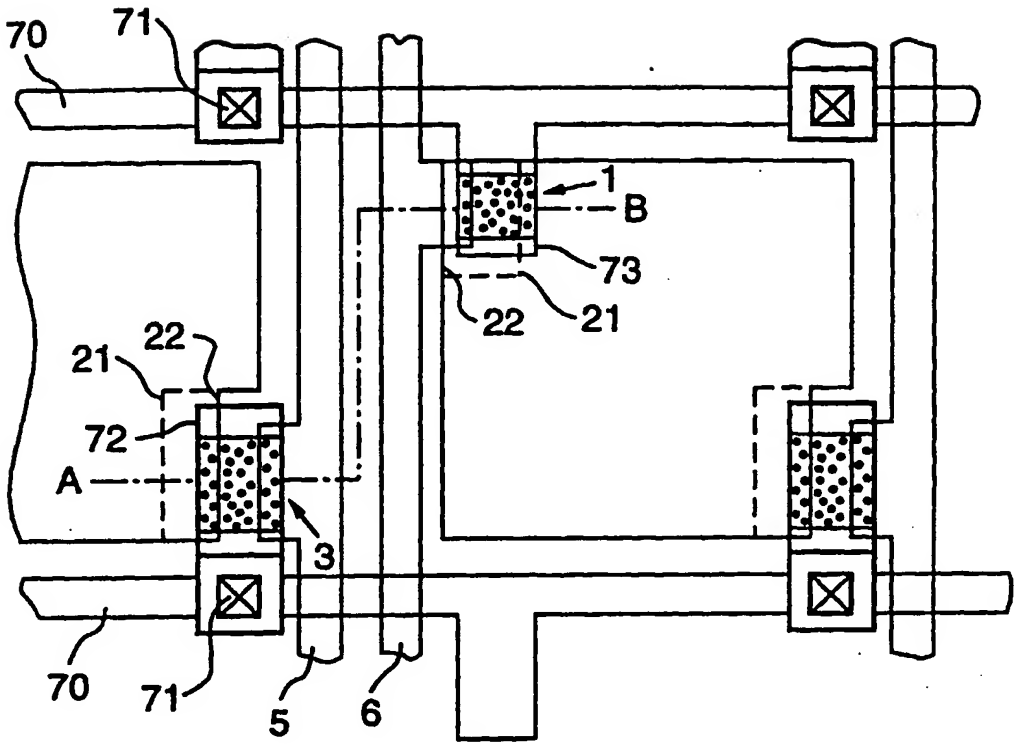

FIG.4.

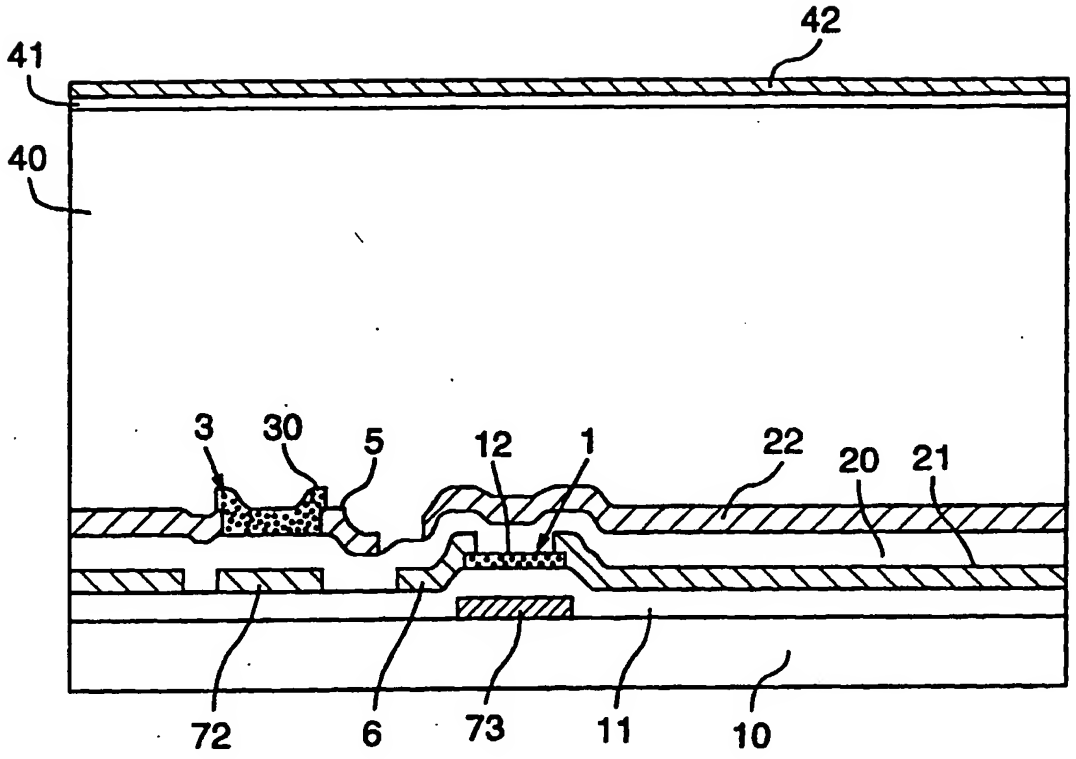

FIG.5.

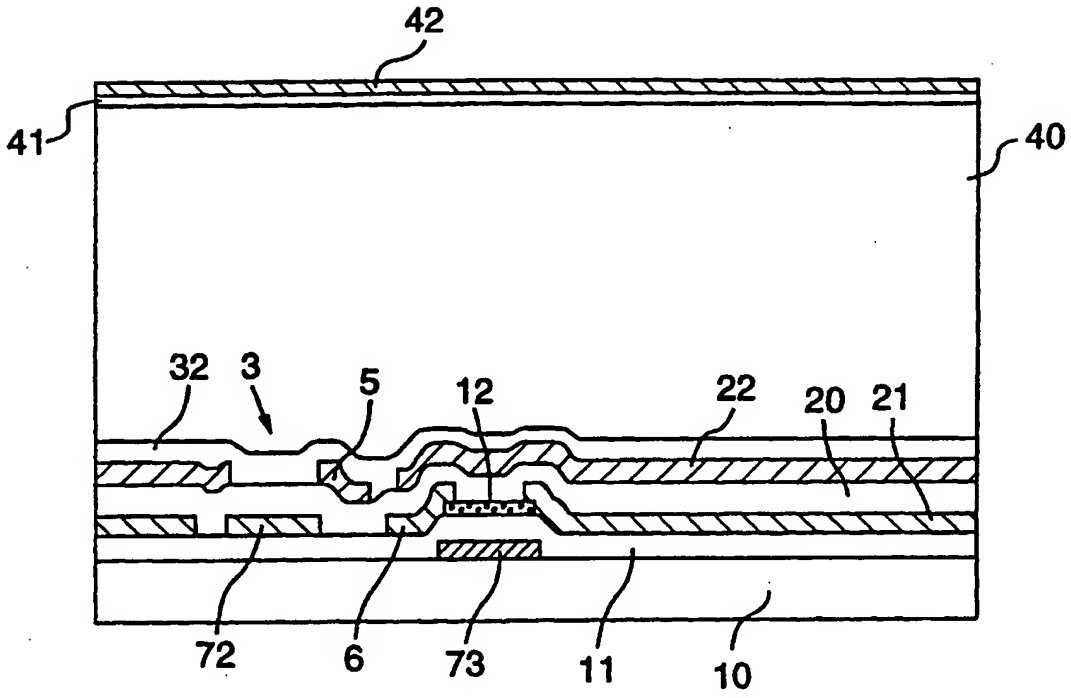

FIG.6.

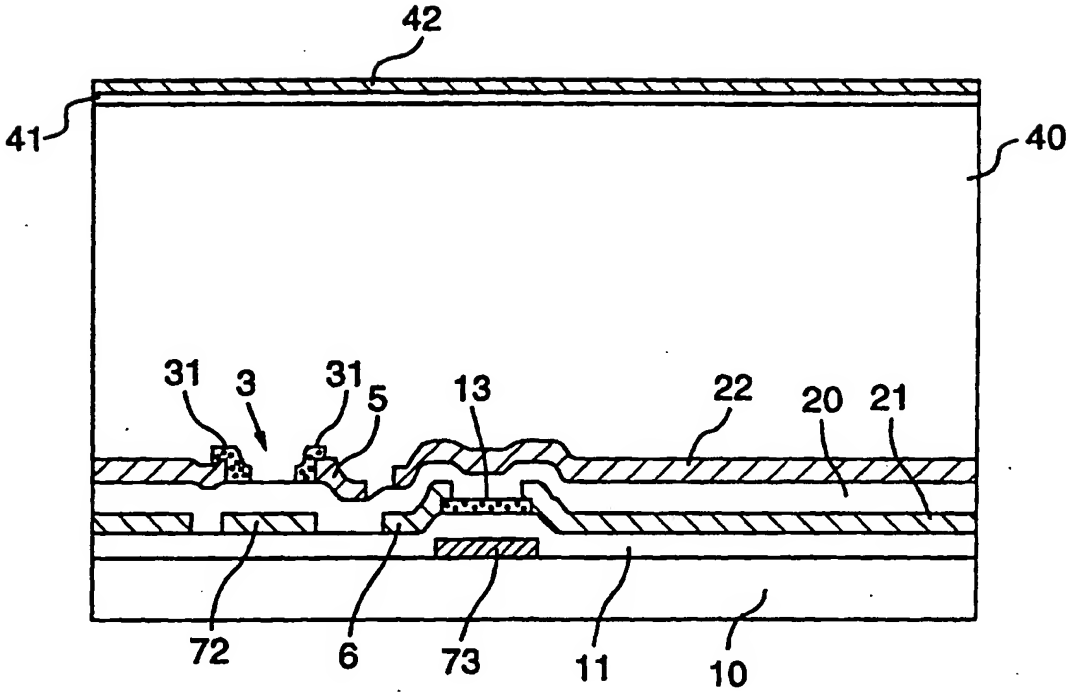

FIG.7.

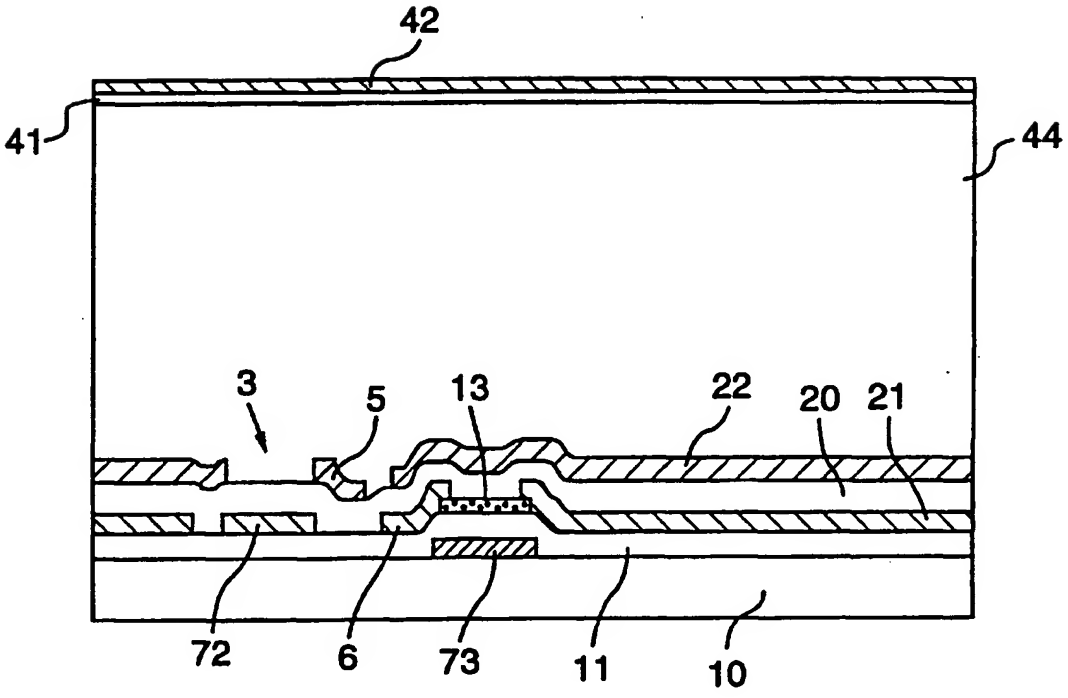

FIG.8.

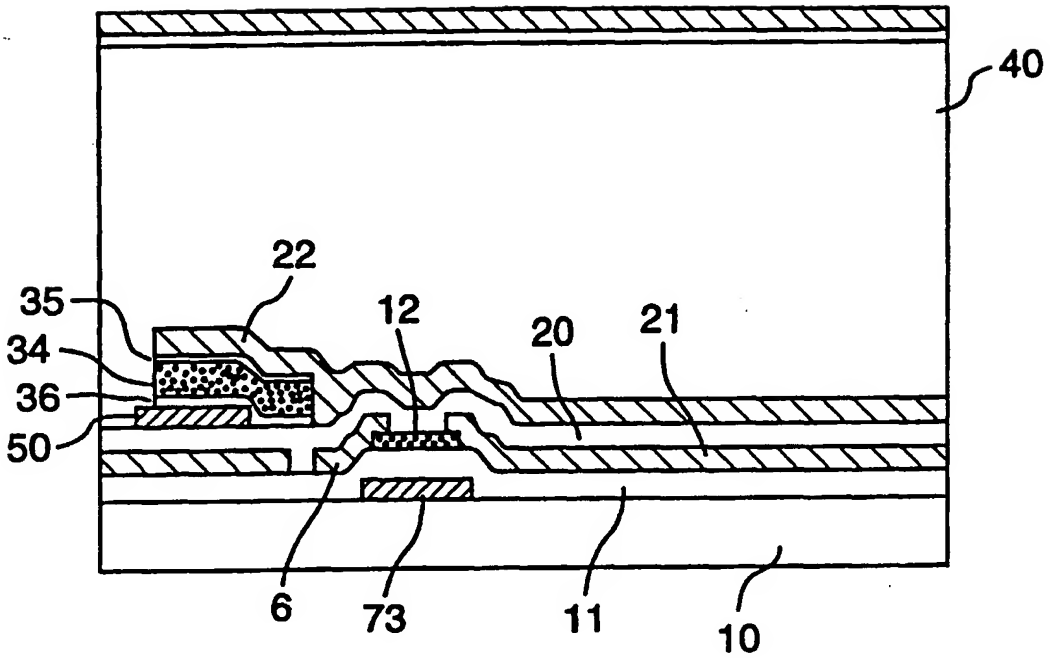

FIG.9.

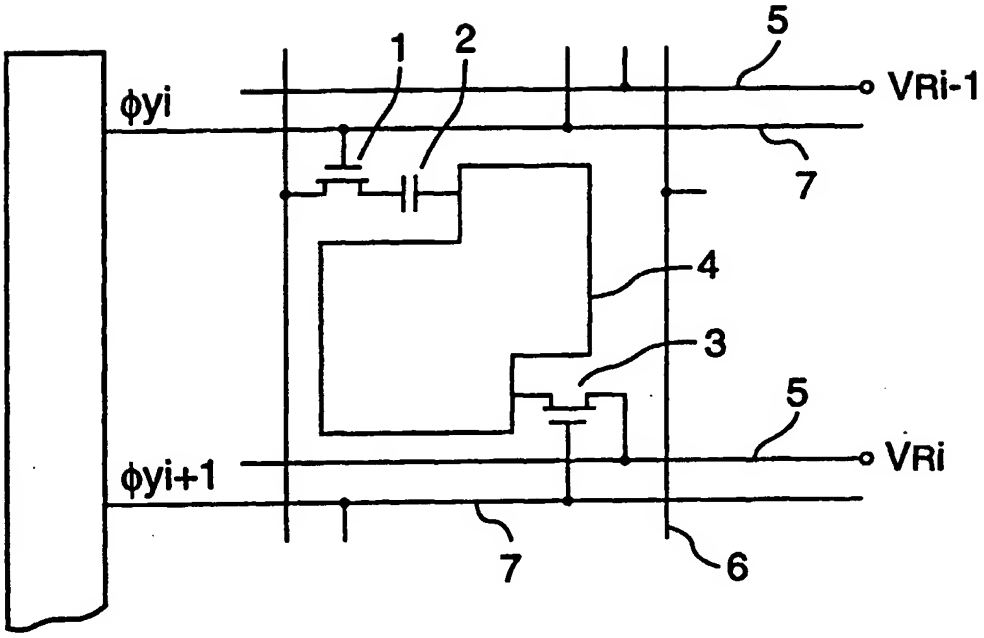

FIG.10.

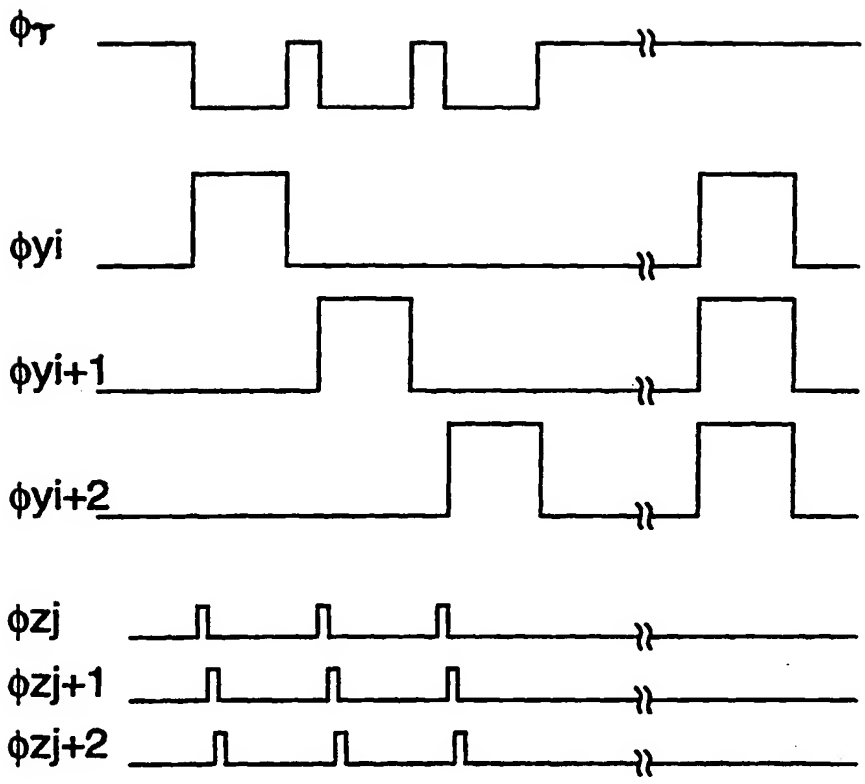

FIG.11.